REMARKS

Claims 10, 11 and 14-16 remain pending. Only claim 10 is being amended hereby.

Claims 10-11 and 14-16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over United States patent application publication no. 2003/0028704 to Mukaida et al. (hereinafter "Mukaida") in view of United States patent application publication no. 2004/0030825 to Otake et al (hereinafter "Otake").

Claims 10-11

It is again respectfully submitted that neither of the cited Mukaida nor Otake references, either alone or in combination, disclose executing write commands received by the flash memory system by either storing the data in parallel in multiple pages of a metablock extending across multiple memory planes or sequentially in blocks of a single plane, depending upon the amount data received with the write commands. Reference is made to the Response to Office Action and Amendment filed October 29, 2007, where this lack of disclosure in the Mukaida and Otake references is discussed in detail.

In response, the current Office Action essentially repeats the obviousness rejection of claim 10 that was previously given and also provides a "Response to Arguments" section on pages 6-8. In that Response, claim 10 is alleged to have been obvious because Mukaida discloses writing data "sequentially into pages within individual blocks of one of the planes," Otake discloses writing data "in parallel into pages within two or more blocks" and the scope of claim 10 is broad enough to read on either of these data write operations alone. In response, claim 10 is being amended to eliminate the "or" when designating these two data write operations, and to more specifically recite the technique. Claim 10 now more clearly recites a method of operating a system that writes data according to one of two data write operations (1) and (2), depending upon the amount to data to be written in response to the write command. The determination of which of the two data write operations is to be performed is further specified to depend upon a number of data units, such as number of data sectors, accompanying a write command that are received with consecutive logical addresses.

Therefore, even if the allegations in the Response section of the Office Action that Mukaida discloses write operation (1) of claim 10 and Otake discloses write operation (2) are

taken to be correct, there is no suggestion of operating the flash memory system by executing one of the claimed write operations (1) and (2) depending upon the amount of data with consecutive logical addresses that are being written by the individual write commands. Claim 10 now more clearly recites operating the memory system by using both of the write operations (1) and (2), something not suggested by the combination of Mukaida and Otake as interpreted in the Office Action.

The Office Action (page 4, lines 12-17) takes the position, however, that it would have been obvious to modify the assumed teachings of Mukaida to write data differently depending upon the amount of data received with an individual host write command "because it improves the performance of writing in flash memories by decreasing evacuation in rewriting." No citation is provided to the references, common knowledge or anything else that indicates an awareness of this problem, let alone that it would have been obvious to solve it by the claimed techniques. By "evacuation" it is assumed that the process that is alternately referred to as "data consolidation" or "garbage collection" was meant. It is noted that the problem described in the Office Action and the use of the claimed method to solve that problem were described in the present application (see the first two paragraphs 0012 and 0013 of the Summary of the Invention, for example), which is of course not prior art. Each of the cited Mukaida and Otake describes its own data writing technique that it says solves different problems. It is of course improper to piece together selected teachings of two references after learning the problem to be solved from the present application.

The foregoing discussion assumes that the Office Action is correct in its description of what Mukaida teaches. Even so, the methods defined by the claims are submitted to have been non-obvious over them. But in addition, it is submitted that Mukaida does not anticipate the data writing option (1) of claim 10, contrary to the position taken in the Office Action. Claim 10 comprises for option (1) writing "all the data received with individual commands . . . in *only one* of the planes" (emphasis added). Mukaida's figure 12, referenced in the Office Action as showing single plane writing, instead shows executing a write command by writing data into *all* of the flash memory chips 2-0 to 2-3. Although written sequentially into one chip at a time, the data are clearly described by Mukaida to be written in all four of its flash memory chips. The

data are therefore not written into individual blocks of *only one* of the planes as specified by claim 10.

Mukaida's figure 22, also referenced in the Office Action, is even further removed from the single plane limitation of claim 10 because it writes data into all four banks #0 – #3 in parallel. Data for each of the banks are loaded into the memory chip in time sequence but once loaded are then flash programmed simultaneously into all the four banks.

Paragraphs 0345-0346 of page 20 of Mukaida, referenced in the Office Action, describe yet a different programming technique that is illustrated in its figure 29. Multiple banks of one flash memory chip are flashed programmed simultaneously, followed by multiple banks of another flash memory chip. This is also submitted to have nothing to do with the claimed alternative of writing data sequentially in only one of the memory planes.

Therefore, for any or all of these reasons, it is respectfully submitted that claim 10, and thus also its dependent claim 11, are patentable over the cited Mukaida and Otake references.

Claims 14-16

Independent claim 14 is believed to be patentable for the same reasons given above for claim 10. Claim 14 specifies the operation of a memory system that stores data either in parallel in more than one sub-array or in a single sub-array, depending upon whether multiple pages or *only a single* page of data are received with the write command. The memory system is defined to operate in either one of these data write modes, depending upon the number of pages of data received with a write command, something that neither of the cited Mukaida or Otake references suggests.

Even if the disclosures of Mukaida or Otake are fit together in some manner, such a combination would not include the option of writing *all* the received data into pages of blocks of *only one* of the sub-arrays when there is a small amount of data being written. Mukaida writes data received with a write command into more than one of its planes, although in only one plane at a time. In Otake, data are written in parallel into two or more blocks. Therefore, similar to what is discussed above with regard to claim 10, claim 14 would distinguish from combining the teachings of Mukaida or Otake.

Dependent claim 15 highlights one of the applications of the method of claim 14 that is quite important . Updating the FAT each time new data are written, or when existing data are updated, typically results in many repetitive single sector or page writes to the memory. This adversely affects the performance of the memory system but the technique of claim 14 overcomes this by treating single page writes differently from multiple page writes. Nothing in either of the cited Mukaida or Otake references has been found to suggest this advantage of single page writes on maintaining FAT data.

In addition, the last paragraph of claim 14 calls for "maintaining indications" associated with the individual written data sectors that indicate whether or not the sector was written into the memory in logical sequence with other sectors. The Office Action (p. 6, lines 3-5) alleges that this is disclosed by Otake, referencing its paragraphs 0059-0064 that describe the block management table of Otake's Figure 3. However, that table provides an entry for each "logical address block" and not for the individual sectors. That table also does not specify that a given sector was written in a single block, as claimed. The table of Otake is not "associated with the written sectors of data" as recited in the last paragraph of claim 14.

Dependent claim 16 calls for storing the indications of the last paragraph of claim 14 in headers of data sectors. The Office Action (page 6, lines 16-17) references paragraph 0308 of Mukaida as describing this. But this paragraph describes the address translation table of Figure 25. No suggestion has been found that any part of this table is stored in the headers of data sectors.

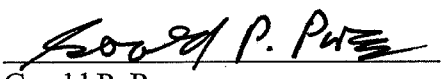
For these reasons, it is respectfully submitted that claim 14 and its dependent claims 15 and 16, are patentable over the cited Mukaida and Otake references.

Conclusion

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned attorney at 415-276-6534 would be appreciated.

FILED VIA EFS

Respectfully submitted,



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